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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,223	12/12/2005	Haruhiko Ikeda	36856.1394	2555

54066 7590 10/17/2007  
MURATA MANUFACTURING COMPANY, LTD.  
C/O KEATING & BENNETT, LLP  
8180 GREENSBORO DRIVE  
SUITE 850  
MCLEAN, VA 22102

EXAMINER
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GREEN, PHILLIP

ART UNIT	PAPER NUMBER
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2823

NOTIFICATION DATE	DELIVERY MODE
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10/17/2007

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

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JKEATING@KBIPLAW.COM  
uspto@kbiplaw.com



## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election without traverse of Specie 1: Figures 1 and 2, including claims 8-12 in the reply filed on August 06, 2007 is acknowledged. Claims 13 - 21 are withdrawn from consideration.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakatani et al (US 6625037) in view of Sugaya et al (US 6931725).

Re claim 8, Sugaya discloses a process for producing a component-embedded substrate, comprising the steps of:

connecting and fixing a first electronic component (304) to a first electrode (303) pattern on a first supporting layer (305) with a conductive bonding material;

press-bonding a second supporting layer (307) including a second electrode pattern (306) onto the electronic component-fixed surface of the first supporting layer (305) with a first prepreg therebetween to perform transfer; (Note: Figure 3F)

separating the first supporting layer (305) and the second supporting layer (307) from the first prepreg such that the first and second electrode patterns (304 and 306) are disposed on a front surface and a back surface of the first prepreg; (Note: Figure 3I)

curing the first prepreg before or after the step of separating the first supporting layer and the second supporting layer from the first prepreg; (Note: Column 17, 1-16)

Although Sugaya discloses a second electronic component, Sugaya does not explicitly disclose the manner used to attach the electronic component.

Nakatani discloses a method of producing a component-embedded substrate. Nakatani connects and fixes a first electronic component to a first electrode pattern on a first supporting layer with a conductive bonding material; press-bonding a resin layer onto the electronic component-fixed surface of the first supporting layer;

connecting and fixing a second electronic component onto a back surface of the second electrode pattern with a conductive bonding material.;

press-bonding a third supporting layer including a third electrode pattern onto a second electronic component-fixed surface with a second prepreg therebetween to perform transfer;

separating the third supporting layer from the second prepreg; and curing the second prepreg before or after the step of separating the third supporting layer from the second prepreg, wherein the prepregs and the electrode patterns are sequentially laminated. (Note: Figure 6).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Sugaya et al. reference with the second component attached, pressed and heated as taught by the Nakatani et al. in order to allow "the epoxy resin in the sheet to be cured, so that the circuit

components and the wiring pattern and the sheet were strongly connected mechanically.” (Note: Column 20, line 38-57).

Re claim 9, as applied to claim 8 in the paragraph above, Nakatani and Sugaya disclose the claimed limitations, including,

forming a through hole in the first prepreg which extends in a thickness direction of the first prepreg after heating the prepreg; and

forming a conducting path inside the through hole, the conducting path electrically connecting the first and second electrode patterns provided on the front surface and the back surface of the first prepreg. (Note: Nakatani, Column 8, line 45 – Column 9, line 62, where Nakatani teaches a temporary curing).

Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955) (Claimed process which was performed at a temperature between 40°C and 80°C and an acid concentration between 25% and 70% was held to be prima facie obvious over a reference process which differed from the claims only in that the reference process was performed at a temperature of 100°C and an acid concentration of 10%.)

Re claim 10, as applied to claim 8 in the paragraph above, Nakatani and Sugaya 131disclose the claimed limitations, including,

Art Unit: 2823

forming a through hole in the first prepreg connecting the electrode pattern provided on the front surface or the back surface of the first prepreg with an external electrode of the first electronic component after heating the first prepreg; and

forming the conducting path inside the through hole, the conducting path electrically connecting the electrode pattern with the external electrode of the first or second electronic component. (Note: Nakatani, Column 8, line 45 – Column 9, line 62 and Figure 6)

Re claim 11, as applied to claim 8 in the paragraph above, Nakatani and Sugaya disclose the claimed limitations, including,

wherein the step of curing the first prepreg further comprises the substeps of: performing temporary curing before separating the first and second supporting layers from the first prepreg; and

performing complete curing after separating the first and second supporting layers from the first prepreg. (Note Sugaya, Figure 3; Nakatani, Column 8, line 45 – Column 9, line 62)

Re claim 12, as applied to claim 8 in the paragraph above, Nakatani and Sugaya disclose the claimed limitations, including,

wherein the step of curing the second prepreg further comprises the substeps of: performing temporary curing before separating the third supporting layer from the second prepreg; and

performing complete curing after separating the third supporting layer from the second prepreg. (Note Nakatani, Figure 6)

***Correspondence***

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phillip S. Green whose telephone number is 571-272-7024. The examiner can normally be reached on Monday thru Thursday 9:30 am to 7:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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10/10/2007

  
BROOK KEBEDE  
PRIMARY EXAMINER